

**Method and Apparatus for Frequency-Robust Detection Of A Wideband Code  
Division Multiple Access Secondary Synchronization Channel**

**FIELD OF THE INVENTION**

The present invention relates to processing of received code division multiple  
5 access ("CDMA") signals.

**BACKGROUND OF THE INVENTION**

This section is intended to introduce the reader to various aspects of art  
which may be related to various aspects of the present invention which are  
10 described and/or claimed below. This discussion is believed to be helpful in  
providing the reader with background information to facilitate a better understanding  
of the various aspects of the present invention. Accordingly, it should be understood  
that these statements are to be read in this light, and not as admissions of prior art.

Manufacturers of wireless communication devices have a wide range of  
15 transmission technologies to choose from when designing wireless systems. Some  
exemplary technologies include time division multiple access ("TDMA"), code  
division multiple access and the like. CDMA, which is typically implemented using  
direct sequence spread spectrum technology, is very popular in communications  
systems, including cellular telephones and the like.

20 In a CDMA system, a code or symbol is assigned to all speech bits in a voice  
signal. The symbols are encoded across a frequency spectrum and transmitted to a  
receiver. When the encoded CDMA symbols are received, they are decoded and  
reassembled into a signal representative of the original voice signal.

In processing received CDMA signals, it may be difficult to detect long  
25 symbols in the presence of a frequency offset. Because the chips (each chip is  
equal to one bit in a spreading code) that make up a symbol may tend to rotate in  
the presence of a frequency offset, it is possible for the chips to rotate completely  
around the complex plane during the integration period of one symbol. When this  
happens, the chips may destructively combine to produce a very small correlation  
30 peak. One method may be to solve this problem may be to implement a frequency  
synchronization block in hardware, but such solutions may be undesirably expensive  
in order to be able to tolerate higher frequency offsets. Absent more expensive  
hardware solutions, a receiver may only be able to detect long symbols in the  
presence of relatively low frequency offsets. An improved method and apparatus for

the detection of long symbols in the presence of a relatively high frequency offset is desirable.

# SUMMARY OF THE INVENTION

5           The disclosed embodiments may relate to a method and apparatus for performing a correlation with respect to a received signal. A first correlator may correlate for a real part of a first characteristic of the received signal to produce a first real correlated signal. A second correlator may correlate for an imaginary part of the first characteristic of the received signal to produce a first imaginary correlated  
10   signal. A third correlator may correlate for a real part of a second characteristic of the received signal to produce a second real correlated signal. A fourth correlator may correlate for an imaginary part of the second characteristic of the received signal to produce a second imaginary correlated signal. Logic may combine a signal that corresponds to the first real correlated signal, a signal that corresponds to the  
15   first imaginary correlated signal, the second real correlated signal and the second imaginary correlated signal to produce a real part of a frequency adjusted signal and an imaginary part of the frequency adjusted signal.

# BRIEF DESCRIPTION OF THE DRAWINGS

20           In the drawings:

FIG. 1 is a block diagram of an exemplary CDMA receiver in which embodiments of the present invention may be employed;

FIG. 2, which comprises FIG. 2A and FIG. 2B, is a block diagram of a Secondary Synchronization Channel correlation block that may be employed in a  
25   cell search block according to an embodiment of the present invention; and

FIG. 3 is a block diagram of a primary synchronization code ("PSC") frequency adjust block in accordance with an embodiment of the present invention.

# DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

30           One or more specific embodiments of the present invention will be described below. In an effort to provide a concise description of these embodiments, not all features of an actual implementation are described in the specification. It should be appreciated that in the development of any such actual implementation, as in any engineering or design project, numerous implementation-specific decisions may be

made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which may vary from one implementation to another. Moreover, it should be appreciated that such a development effort might be complex and time consuming, but would nevertheless be a routine undertaking of design, fabrication, and manufacture for those of ordinary skill having the benefit of this disclosure.

FIG. 1 is a block diagram of an exemplary CDMA receiver in which embodiments of the present invention may be employed. The CDMA receiver is generally referred to by the reference numeral 10. After an analog CDMA signal is received, it is converted to a digital signal by an analog-to-digital converter 12. The digital output of the analog-to-digital converter 12 is delivered to a matched filter 14. The matched filter 14 produces a signal that matches the shape of the transmitted signal.

The output of the matched filter 14 is delivered to a tapped delay line 16, which provides output to various receiver components. The various taps of the tapped delay line 16 may be adjusted to synchronize the operation of the CDMA receiver 10.

One output from the tapped delay line 16 is delivered to a cell search block 18. The cell search block may be implemented in receivers that comply with third generation ("3G") wireless communication standards such as the Universal Mobile Telecommunications System ("UMTS") Wideband Code Division Multiple Access ("WCDMA") standard, which is hereby incorporated by reference, to synchronize a mobile terminal such as a cellular telephone with a base station. The cell search block 18 may perform synchronization when a user's phone is first turned on or when synchronization with the base station is lost (for example, after going through a tunnel).

In the UMTS WCDMA standard, both the Primary Synchronization Channel ("SCH") and Common Pilot Channel ("CPICH") have a length of 256 chips. The Primary SCH channel is a sparse channel and it only contains data during the first 256 chips of each 2560 chip slot. The same data is repeated for every slot in the frame and all frames carry the same Primary SCH channel. In addition, all cells in a WCDMA system transmit identical Primary SCH channels. Once the Primary SCH channel is acquired by a mobile terminal, the receiver will have achieved chip, symbol and slot synchronization. However, since the Primary SCH contains the

same data in every slot, it cannot be used to achieve frame synchronization because all slots in a frame are identical and hence they cannot be used to determine the location of the frame start.

5 The sign of the data on the SCH channel (both Primary and Secondary SCH) is used to indicate to the mobile terminal whether or not space-time transmit diversity ("STTD") encoding is being used on the downlink Primary Common Control Physical Channel ("P-CCPCH"). The polarity of the SCH channel does not affect the cell search process since the algorithms only process the magnitude of the correlations of the signal.

10 The signal transmitted on the Primary SCH channel is called the Primary Synchronization Code ("PSC") and it is constructed from a hierarchical Golay sequence. This sequence was chosen because it has good aperiodic autocorrelation properties. Another desirable feature of the sequence is that a low-complexity matched filter can be used to process it. The reduced complexity of the  
15 matched filter is possible because of the hierarchical nature of the sequence.

The Secondary SCH channel is different for every cell in a UMTS system and its purpose is to aid the receiver in obtaining frame synchronization as well as knowledge of the scrambling code group used in the current cell. Like the Primary SCH channel, the Secondary SCH channel is also only transmitted during the first  
20 256 chips of each slot. Each slot of a frame contains a Secondary Synchronization Code ("SSC"). There are a total of 16 possible SSCs. These SSCs are complex-valued and they are based on Hadamard sequences.

The CPICH is a continuous downlink pilot signal that contains a known training sequence scrambled by the current cell's scrambling code. The training  
25 sequence used is a constant  $1+j$ . Unlike the SCH channel, the CPICH is a continuous signal that is transmitted for the entire duration of each frame. Once the correct scrambling code group is determined, the receiver can correlate against the CPICH using each of the eight different scrambling codes in a given code group in order to find the correct scrambling code for the current cell.

30 The cell search block 18 performs at least two functions. First, it acquires the Primary SCH channel to achieve slot synchronization. A UMTS frame (with duration of 10 ms) consists of 38400 chips. The frame is made up of 15 slots, each of 2560 chips in length. After the cell search block 18 acquires slot synchronization, the CDMA receiver 10 has knowledge of slot boundaries, but it still does not know when

frames start. Second, the cell search block 18 then acquires the Secondary SCH channel in order to achieve frame synchronization.

Simultaneously, the acquisition of the Secondary SCH channel uniquely determines which downlink scrambling code group is being transmitted. Each code group contains eight possible scrambling codes and the block correlates against each one to determine which one has the highest peak (and hence the most likelihood of being transmitted). Once determined, other blocks in the CDMA receiver 10 can tune to the base station by using this scrambling code. The identification of the Secondary SCH channel by the cell search block 18 is described in greater detail below with reference to FIGs. 2 and 3.

The tapped delay line 16 delivers a second output to a searcher block 20. A scrambling code generator 26 also delivers a signal to the searcher block 20. The searcher block 20 correlates the received samples against different delayed versions of the scrambling code. By monitoring the correlation outputs at different offsets of the scrambling code, the block searches for peaks which represent multipath signals on which the receiver can receive data.

A plurality of 1-N finger circuits 22, 24 may be included in the CDMA receiver 10. The finger circuits 22, 24 may receive input from the tapped delay line 16, the scrambling code generator 26 and a spreading code generator 28. In a spread-spectrum CDMA system such as required by UMTS, data bits are used to modulate spreading codes of different lengths. If a bit is modulated onto a spreading code of length 256, the data rate will be low (because it takes 256 chips to send a bit) but the processing gain will be high (because of the correlation gain from correlating against a sequence of length 256). If a bit is modulated onto a spreading code of length four, the data rate will be high (because a bit can be sent every four chips) but the processing gain will be low (since there is not much correlation gain from correlating against a short four-chip sequence).

Each of the finger circuits 22, 24 may be dropped onto a peak found by the searcher block 20. Each of the finger circuits 22, 24 may contain a correlator that correlates the received samples against the scrambling code delayed by a given amount. The finger circuits 22, 24 may despread the data.

The output of the finger circuits 22, 24 is delivered to a maximal ratio combiner ("MRC") 30. The MRC 30 takes the samples from each finger (which corresponds to different multipath versions of the same downlink transmitted signal),

rotates them by their pilots to align the phase of the signals and adds them together to form the estimate of the transmitted symbols that will be processed by the CDMA receiver 10.

5 The outputs of the cell search block 18, the searcher block 20 and the MRC 30 may be delivered to an embedded processor (not shown) for further processing. As set forth above, FIG. 2 further illustrates the operation of the cell search block 18 to correlate the Secondary SCH channel in a received WCDMA signal.

FIG. 2, which comprises FIG. 2A and FIG. 2B, is a block diagram of a Secondary SCH correlation block that may be employed in a cell search block  
10 according to an embodiment of the present invention. The Secondary SCH correlation block is generally referred to by the reference numeral 100 in both FIGs. 2A and 2B. The Secondary SCH correlation block 100 may use the output of a correlation for the Primary SCH channel to derive a frequency adjustment that is applied prior to the second stage of correlation for the Secondary SCH channel.  
15 Thus, the Secondary SCH detection algorithm may work under much higher frequency offsets than would otherwise be possible.

Beginning with FIG. 2A, the Secondary SCH correlation block 100 comprises a clock signal 102 to synchronize its operations. Also included is a reset signal 104,  
20 which may be used to reset the Secondary SCH correlation block 100, for example, upon initialization.

The Secondary SCH channel is designed as a hierarchical sequence. Reception of that channel is accomplished by first correlating against one of the hierarchical sequences. The output of that correlator is then correlated against the second hierarchical sequence. Typically, the first correlation is for the *b* sequence  
25 of the Secondary SCH channel (defined in the UMTS WCDMA standard), and the second correlation is for the *H<sub>z</sub>* sequence (defined in the UMTS WCDMA standard).

A down sample block 106 receives a received sample (for example, from the tapped delay line 16 (FIG. 1)). The received sample may comprise a real part (*rx\_samp\_re*) and an imaginary part (*rx\_samp\_im*). The real portion  
30 (*downsample\_re*) of the output of the downsample block 106 is delivered to a PSC correlator 108 and a SSC *b* correlator 114. The imaginary portion (*download\_im*) of the output of the downsample block 106 is delivered to a PSC correlator 110 and a SSC *b* correlator 116. The output of the PSC correlator 108 (*psc\_corr\_re*) and the

output of the PSC correlator 110 (psc\_corr\_im) are delivered to a PSC frequency adjust block 112.

The output of the PSC frequency adjust block 112, which comprises a real part (freq\_adj\_re) and an imaginary part (freq\_adj\_im), is delivered to a multiplier 118. The outputs of the SSC *b* correlator 114 and the SSC *b* correlator 116 are also delivered to the multiplier 118.

The PSC correlators 108 and 110 correlate against the *a* sequence of the Primary SCH channel (defined in the UMTS WCDMA standard). This correlation occurs simultaneously with the operation of the SSC *b* correlators 114 and 116. The PSC frequency adjust block 112 computes complex-valued samples (one for every SSC *b* sequence correlation period) that is multiplied by the outputs of the SSC *b* correlators by the multiplier 118 before the output of the multiplier 118 is delivered for processing by SSC Hz correlators (see FIG. 2B). This adjustment factor rotates the samples in order to correct for the rotation due to the frequency offset.

Turning to FIG. 2B, a real part (mult\_re) of output of the multiplier 118 is delivered to a SSC Hz correlator 120 and an imaginary part (mult\_im) of the output of the multiplier 118 is delivered to a SSC Hz correlator 122. The output of the SSC Hz correlator 120 (psc\_corr2\_re) and the output of the SSC Hz correlator 122 (psc\_corr2\_im) are delivered to a non-coherent combiner 124. The output of the non-coherent combiner 124 (combiner\_out) is delivered to a frame buffer accumulator 126.

The output of the frame buffer accumulator 126 (accum\_out) is delivered to a SSC peak locator 128. The output of the SSC peak locator 128 (ssc\_peaks) is delivered to a SSC peak detector 130. The SSC peak detector 130 provides a scram\_code\_group output and a slot\_offset output, which are used for further processing.

FIG. 3 is a block diagram of a PSC frequency adjust block in accordance with an embodiment of the present invention. The PSC frequency adjust block shown in FIG. 3 corresponds to the PSC frequency adjust block 112 (FIG. 2), so it is referred to by the reference numeral 112.

The PSC frequency adjust block 112 receives the psc\_corr\_re signal from the PSC correlator 108 and the psc\_corr\_im signal from the PSC correlator 110. The psc\_corr\_re signal is delivered to a complex multiply block 204. The psc\_corr\_im signal is delivered to a sign flip block 202, which determines the complex conjugate

of the psc\_corr\_im signal. The output of the sign flip block 202 is delivered to the complex multiply block 204. The complex multiply block 204 multiplies the received signals by a stored second layer of the PSC sequence 206. That stored sequence may comprise 16 samples, as shown in FIG. 3.

5 The real output of the complex multiply block 204 corresponds to the freq\_adj\_re signal shown in FIG. 2A. An imaginary part of the output of the complex multiply block 204 is delivered to a sign flip block 208, which takes its complex conjugate. The output of the sign flip block 208 corresponds to the freq\_adj\_im signal shown in FIG. 2A.

10 While the invention may be susceptible to various modifications and alternative forms, specific embodiments have been shown by way of example in the drawings and will be described in detail herein. However, it should be understood that the invention is not intended to be limited to the particular forms disclosed. Rather, the invention is to cover all modifications, equivalents and alternatives falling  
15 within the spirit and scope of the invention as defined by the following appended claims.